In The Claims:

Claim 1. (currently amended) A re-oxidation process of a semiconductor device, comprising:

providing a substrate having a stacked structure thereon, wherein the stacked structure includes a polysilicon/tungsten silicide interface;

forming a CVD oxide layer on both the substrate and the stacked structure with a chemical vapor deposition (CVD) process; and

performing an oxidation process to form a thermal oxide layer on both the substrate and the stacked structure.

Claim 2. (original) The re-oxidation process of claim 1, wherein the stacked structure includes a stacked gate that comprises, from bottom to top, a tunneling layer, a polysilicon floating gate, an inter-poly dielectric layer, a polysilicon control gate and a tungsten silicide layer.

Claim 3. (original) The re-oxidation process of claim 1, wherein the stacked structure includes a stacked gate that comprises, from bottom to top, a gate dielectric layer, a polysilicon gate and a tungsten silicide layer.

Claim 4. (original) The re-oxidation process of claim 1, wherein the CVD process is a low-pressure chemical vapor deposition (LPCVD) process or a plasma-enhanced chemical vapor deposition (PECVD) process.

Claim 5. (original) The re-oxidation process of claim 1, wherein the CVD oxide layer is formed using silane (SiH_4), tetraethyl-ortho-silane (TEOS) or dichlorosilane (SiH_2Cl_2) as a Si-source.

Claim 6. (original) The re-oxidation process of claim 1, wherein the CVD oxide layer has a thickness from 30Å to 120Å.

Claim 7. (original) The re-oxidation process of claim 1, wherein the oxidation process is conducted under O_2, H_2O or O_2/H_2O atmosphere.

Claim 8. (original) The re-oxidation process of claim 1, wherein the oxidation process is conducted in a batch-type or single wafer-type reaction chamber.

Claim 9. (currently amended) A method for fabricating a semiconductor device, comprising:

sequentially forming a tunneling layer, a first polysilicon layer, an inter-poly dielectric layer, a second polysilicon layer and a tungsten silicide layer on a substrate;

sequentially patterning the tungsten silicide layer, the second polysilicon layer, the inter-poly dielectric layer and the first polysilicon layer to form a stacked gate;

forming a CVD oxide layer on both the substrate and the stacked gate with a chemical vapor deposition (CVD) process; and

performing an oxidation process to form a thermal oxide layer on both the substrate and the stacked gate.

Claim 10. (original) The method of claim 9, wherein the CVD process is a low-pressure chemical vapor deposition (LPCVD) process or a plasma-enhanced chemical vapor deposition (PECVD) process.

Claim 11. (original) The method of claim 9, wherein the CVD oxide layer is formed using silane (SiH_4), tetraethyl-ortho-silane (TEOS) or dichlorosilane (SiH_2Cl_2) as a Si-source.

Claim 12. (original) The method of claim 9, wherein the CVD oxide layer has a thickness from 30Å to 120Å.

Claim 13. (original) The method of claim 9, wherein the oxidation process is conducted under O_2, H_2O or O_2/H_2O atmosphere.

Claim 14. (original) The method of claim 9, wherein the oxidation process is conducted in a batch-type or single wafer-type reaction chamber.

Claim 15. (currently amended) A re-oxidation process of a semiconductor device, comprising:

providing a substrate having a stacked structure thereon, wherein the stacked structure includes a polysilicon/metal silicide interface;

forming a CVD oxide layer on both the substrate and the stacked structure with a chemical vapor deposition (CVD) process; and

performing an oxidation process to form a thermal oxide layer on both the substrate and the stacked structure.

Claim 16. (original) The re-oxidation process of claim 15, wherein the stacked structure includes a stacked gate that comprises, from bottom to top, a tunneling layer, a polysilicon floating gate, an inter-poly dielectric layer, a polysilicon control gate and a metal silicide layer.

Claim 17. (original) The re-oxidation process of claim 15, wherein the stacked structure includes a stacked gate that comprises, from bottom to top, a gate dielectric layer, a polysilicon gate and a metal silicide layer.

Claim 18. (original) The re-oxidation process of claim 15, wherein the CVD process is a low pressure chemical vapor deposition (LPCVD) process or a plasma enhanced chemical vapor deposition (PECVD) process.

Claim 19. (original) The re-oxidation process of claim 15, wherein the CVD oxide layer is formed using SiH_4, tetraethyl-ortho-silane (TEOS) or dichlorosilane (SiH_2Cl_2) as a Si-source.

Claim 20. (original) The re-oxidation process of claim 15, wherein the CVD oxide layer has a thickness from 30Å to 120Å.